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Press release

Codasip collaborates with Siemens to deliver trace solution for custom processors

Significant productivity gains even in the most complex heterogeneous and custom designs

Munich, Germany, 5 September 2023 – Codasip®, the leader in RISC-V Custom Compute, now offers the Tessent™ Enhanced Trace Encoder solution from the Tessent Embedded Analytics product line at Siemens EDA with its customizable RISC-V cores. Through the joint solution, developers can efficiently trace and debug issues between silicon and software, and accurately understand real-time behaviors of even the most complex customized designs based on Codasip RISC-V processors™.

Codasip RISC-V processors are fully customizable and adaptable to the unique needs of an application. System designers can use the Codasip Studio™ toolchain to find the best software and hardware trade-offs and achieve optimal features and PPA (Power, Performance, Area). The combination of customizable processors and tools for processor design enables an automated approach to achieve Custom Compute. To make this customization usable for software developers, Codasip makes sure that all tools—including the compiler and debugger—also support customization. This now includes the trace solution.

Including trace in an SoC significantly speeds up the time-consuming software debug task and hereby reduces the bring-up time and the cost of software development. Codasip has chosen to work with Siemens EDA for its Trace Encoder because the companies share a belief in product quality achieved efficiently throughout the whole product design flow. This focus on quality empowers innovation and delivers significant productivity gains for customers even in the most complex heterogeneous and custom designs.

The Tessent Enhanced Trace Encoder builds on the RISC-V standard produced by the Debug and Trace Working Group, which was led by representatives from Siemens who donated the Trace algorithm to the RISC-V International community. However, the solution from Siemens goes well beyond the RISC-V standard, offering a far more efficient tool with significant productivity gains in the development of the most complex systems, and it supports custom instructions. It conducts detailed examinations on systems to find the bug and its root cause. It is cycle-accurate, which means the developer gets insights into each and every instruction.

Mike Eftimakis, VP Strategy and Ecosystem, Codasip, commented, “Codasip has high standards of quality when it comes to our processor IP. To ensure this results in outstanding systems, we wanted a trace solution that went much further than the RISC-V standard. The Tessent Enhanced Trace Encoder is optimized for exactly the types of complex and custom systems our customers are developing.”

“Tessent Embedded Analytics enables system-wide real-time debug and post-deployment analytics, helping SoC providers focus on the key task of producing high-quality, innovative products, and getting them to market quickly,” says Ankur Gupta, VP and GM of Siemens EDA’s Tessent division. “Codasip has an outstanding reputation for assisting customers with just these kinds of requirements, and we’re delighted to be working together.”

Codasip will offer the Tessent Enhanced Trace Encoder solution directly to customers to streamline contractual complexity.

About Codasip

Codasip is a processor technology company enabling system-on-chip developers to differentiate their products for competitive advantage. Customers leverage the transformational potential of the open RISC-V ISA in a unique way through Codasip’s custom compute offering: Codasip Studio design automation tools and a fully open architecture licensing model combine with a range of processor IP that can be easily customized. The company is proudly European and serves a global market, where billions of devices are already enabled by Codasip technology. Learn more at www.codasip.com

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